REMARKS

This Amendment is submitted in response to the Office Action dated May 6, 2004, having a shortened statutory period set to expire August 6, 2004. Claims 1-2, 4-6, 8-10, and 12 have been amended, claims 3, 7 and 11 have been cancelled, and claims 13-15 have been added.

Amendments to the Specification:

The specification, on page 1, has been amended to include the U.S. Patent Application Numbers of the related and cross-referenced patent applications.

Claim Rejections Under 35 U.S.C. § 112:

Claims 1-12 have been rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement, namely that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make or use the invention. The substantive support for these rejections is the assertion that "[t]he claims are divorced from the teachings of how the signal is overridden during simulation." Applicants disagree that the original claims were divorced from the teachings of how the signal override occurs during simulation. Referring particularly to Figures 4A-4D and 13B-13C, ample enabling support for the manner in which the inventive method and system performs signal override is explained and depicted. Figures 4A-4C depicts declaring design and instrumentation entity signal ports and how such ports instantiated during HDL compilation and model build (see page 33, line 26 through page 34, line 11, and page 39, line 23 through page 43, line 15). Enabling support for instantiating an override signal port, declaring a signal override during simulation, and selecting the override signal using signal selection means in response to the override declaration is amply provided particularly with reference to Figures 13A-13C. Specifically, on page 91, lines 19-21, it is explained that the signal override port may be declared explicitly as ports in the HDL source code file (see Figure 4C input and output port mapping statements 1364 and 1362 and input and output port mapping statements 1360 and 1361). The declaration of a signal override as the trigger for selecting the override signal is explained with reference to Figures 13B and 13C on page 95, line 10 through page 96 line 3 (explaining that that signal output port mapping logic and connectivity depicted in FIG. 13B is performed by the instrumentation load tool in processing a signal override output declaration 1361).

The foregoing traversal of the rejections under 35 U.S.C. § 112, first paragraph, notwithstanding, claims 1-2, 4-6, 8-10, and 12, as amended, and newly added claims 13-15 are clearly supported by and consistent with the specification teachings of how signal override is facilitated in a hardware description language simulation model as explained in further detail below.

Claims 1, 3, 5, 7 and 9 have been rejected under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter Applicants regard as the invention. In support of these rejections, it is asserted that since no function is specified by the words preceding the word "means," it is impossible to determine the equivalents of the element. Applicants disagree with the basis for these rejections. Claims 3 and 7 have been cancelled rendering their disposition moot. As used in newly added claims 13-15 and amended claims 2, 4, 6, 8, 10 and 12, the word "means" is preceded by the clearly functional terms "signal selection" to form the phrase "signal selection means" (i.e. means for selecting a signal(s)). Such "signal selection means" unambiguously entail the multiplexer MUX 1308 and associated control inputs depicted and described with reference to Applicants' Fig. 13B. Applicants therefore contend that the functional equivalent of "signal selection means," as used in amended claims 2, 4, 6, 8, 10 and 12 and newly added claims 13-15, is clearly described and depicted.

Claim Rejections Under 35 U.S.C. § 102:

Claims 1-12 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,805,792 issued to Swaboda et al. (hereinafter *Swaboda*). In support of these rejections, the Examiner cites col. 2, line 65 (describing a desire for improved emulation, simulation and testability architectures and methods), and col. 26, lines 5-26 (describing an OR gate override mechanism wherein a parallel-configured signal OR gate node input set to logic one overrides the alternate individual OR gate inputs) as disclosing each of the elements of the original claims 1-12. Applicants have amended independent claims 1, 5 and 9 in an effort to more clearly characterize and distinguish Applicants' proposed invention from the subject matter disclosed by *Swaboda*.

As explained in Applicants' Background and on page 91, lines 4-17, overriding signals, in the sense of replacing an original signal with another signal or a processed variation of itself,

is particularly useful during simulation testing of HDL models. Important to Applicants' proposed method and system for providing such simulation testing signal override capacity is the nature and function of "instrumentation entities." As explained in the figures, and particularly with reference to Figures 4B-4D and Figures 13A-13D, Applicants' proposed invention is directed to leveraging comment syntax such that the HDL compiler can distinguish between "design entities" (i.e. HDL entities included in the digital circuit or system that is the object of simulation testing) and "instrumentation entities" (i.e. HDL entities utilized to perform facilitate the testing of the entities incorporated in the digital circuit design). U.S. Pat. No. 6,195,627, commonly owned by the assignee of the present invention, claims an invention wherein a non-conventional comment is utilized to associate an instrumentation entity with a target design entity to be monitored.

The present invention provides a mechanism by which a signal originating from the simulation model may be replaceably overridden in a manner that leverages the use of non-conventional comment syntax to maintain instrumentation entity independence of the design entities. To this end, independent claim 1 has been amended to recite a method for facilitating a signal override in an HDL simulation model in a manner that prevents the instrumentation entity that generates the replacement override signal, from being compiled by the HDL compiler into the digital circuit logic being tested. Specifically, claim 1 recites a method for facilitating signal override in a simulation model of a digital circuit design that includes one or more design entities described utilizing a hardware description language (HDL), said method comprising:

instantiating an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax, said non-conventional HDL comment syntax processed by a post-compiler instrumentation load tool to instantiate said instrumentation entity during a post-compile model build process, wherein said non-conventional HDL comment syntax is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including:

an input port mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden; and

an output port mapping field comprising an override signal field specifying the name of said override signal, a port name field specifying the name of the port from

which said override signal is output from said instrumentation entity, and a target signal field specifying the name of said designated signal to be overridden.

Independent system claim 5 and program product claim 9 have similarly been amended to substantially include the foregoing limitations. Ample support for the foregoing limitations is provided in the Applicants' specification with reference to Figs. 4B-4D and Figs. 13A-13D.

While disclosing various techniques and features for facilitating computer-aided simulation and testability architectures, *Swaboda* fails to disclose or suggest any type of HDL instrumentation entity that is described using comment syntax such that the entity is only post-compile instantiated in the model. Furthermore, nothing in *Swaboda* or any other prior art known to Applicants discloses or suggests a mechanism by which a signal originating from the simulation model may be replaceably overridden in a manner that leverages the use of non-conventional comment syntax to maintain instrumentation entity independence of the design entities. Applicants therefore submit that the amended and newly added claims are patentably distinct from *Swaboda* and a Notice of Allowance to that effect is hereby respectfully requested.

Applicants invite the Examiner to contact the undersigned attorney of record at (512) 343-6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,

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